# Lab 09 – Worksheet

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## Task a. 4:1 MUX

Complete the truth table provided in Table 9.2. As an example, when the Select line input is S1:0=00, output will be the binary number stored in A3:0

Table 9.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |
| 0 | 0 | 0111 | X | X | X | 0111 |
| 0 | 1 | X | 0001 | X | X | 0001 |
| 1 | 0 | X | X | 1001 | X | 1001 |
| 1 | 1 | X | X | X | 0000 | 0000 |

*Provide appropriately commented code for designed module*

|  |
| --- |
| `timescale 1ns / 1ps  module mux\_4\_1(  input [1:0] S,  input [3:0] A,  input [3:0] B,  input [3:0] C,  input [3:0] D,  output [3:0] Y  );  assign Y[3:0] = (S == 2'b00) ? A[3:0] : (S == 2'b01) ? B[3:0] : (S == 2'b10) ? C[3:0] : D[3:0];  endmodule |

*Write a testbench to thoroughly test designed mux\_4\_1 module.*

|  |
| --- |
| `timescale 1ns / 1ps  module testbench\_mux\_4\_1();  reg[1:0] S;  reg[3:0] A;  reg[3:0] B;  reg[3:0] C;  reg[3:0] D;  wire[3:0] Y;  mux\_4\_1 test\_mux\_4(S, A, B, C, D, Y);  initial begin  A [3:0] = 4'b0111;  B [3:0] = 4'b0001;  C [3:0] = 4'b1001;  D [3:0] = 4'b0000;  #100 S = 2'b00;  #100 S = 2'b01;  #100 S = 2'b10;  #100 S = 2'b11;  end  endmodule |

*Attach screenshot of Simulation output- make sure to scale properly for visibility of all case.*

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## Task b. 1:4 DEMUX

Complete the truth table provided in Table 9.4. As an example, when the Select line input is S1:0=00, output EnA will be 0 and the rest of the outputs will remain high.

Table 9.4

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| X | X | 1 | 1 | 1 | 1 | 1 |

*Provide appropriately commented code for designed module*

|  |
| --- |
| `timescale 1ns / 1ps  module DeMux(  input [1:0] S,  input En,  output EnA,  output EnB,  output EnC,  output EnD  );  assign EnA = (S == 2'b00) ? 1'b0 : 1'b1;  assign EnB = (S == 2'b01) ? 1'b0 : 1'b1;  assign EnC = (S == 2'b10) ? 1'b0 : 1'b1;  assign EnD = (S == 2'b11) ? 1'b0 : 1'b1;  endmodule |

*Add your testbench here*

|  |
| --- |
| *`timescale 1ns / 1ps*  *module testbench\_DeMux();*  *reg[1:0] S;*  *reg En;*  *wire EnA;*  *wire EnB;*  *wire EnC;*  *wire EnD;*  *DeMux test(S, En, EnA, EnB, EnC, EnD);*  *initial begin*  *#100 S = 2'b00; En = 1'b0;*  *#100 S = 2'b01; En = 1'b0;*  *#100 S = 2'b10; En = 1'b0;*  *#100 S = 2'b11; En = 1'b0;*  *#100 S = 2'b00; En = 1'b1;*  *end*  *endmodule* |

*Attach screenshot of waveform results here*

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|  |

## Exercise

Write a Verilog module topLevelModule that combines MUX (**mux\_4\_1**) and DeMUX (**demux\_1\_4**) modules created in this lab and binary-hexadecimal decoder module already created in Lab 6, according to the block diagram of Figure 9.2 Top Level Module. This module’s inputs includes four 4-bit data lines (i.e., A[3:0], B[3:0], C[3:0], D[3:0]), 2-bit select line (i.e. S[1:0]) to select from the data for binary-hexadecimal decoder, and a 1-bit active low enable signal (i.e. En). The modules output includes one 7-bit data line for seven segments (i.e., Y [6:0]) and four 1-bit Enable signals (i.e., EnA, EnB, EnC, EnD).

*Provide appropriately commented code for your design module*

|  |
| --- |
| `timescale 1ns / 1ps  module topLevelModule(  input [1:0] S,  input [3:0] A,  input [3:0] B,  input [3:0] C,  input [3:0] D,  output [6:0] Y,  input En,  output EnA,  output EnB,  output EnC,  output EnD  );  wire [3:0] Mux\_out;  mux\_4\_1 m1(S, A, B, C, D, Mux\_out);  segment\_decoder sd1(Mux\_out, Y);  DeMux dm1(S, En, EnA, EnB, EnC, EnD);  endmodule |

*Add your testbench here*

|  |
| --- |
| *`timescale 1ns / 1ps*  *module testbench\_topLevelModule();*  *reg[1:0] S;*  *reg[3:0] A; reg[3:0] B; reg[3:0] C; reg[3:0] D; wire[6:0] Y;*  *reg En; wire EnA, EnB, EnC, EnD;*  *topLevelModule test(S, A, B, C, D, Y, En, EnA, EnB, EnC, EnD);*  *initial begin*  *#100 S = 2'b00; A = 4'b0111; B = 4'b0001; C = 4'b1001; D = 4'b0000; En = 1'b0;*  *#100 S = 2'b01; A = 4'b0111; B = 4'b0001; C = 4'b1001; D = 4'b0000; En = 1'b0;*  *#100 S = 2'b10; A = 4'b0111; B = 4'b0001; C = 4'b1001; D = 4'b0000; En = 1'b0;*  *#100 S = 2'b11; A = 4'b0111; B = 4'b0001; C = 4'b1001; D = 4'b0000; En = 1'b0;*  *#100 S = 2'b00; A = 4'b0111; B = 4'b0001; C = 4'b1001; D = 4'b0000; En = 1'b1;*  *end*  *endmodule* |

*Attach screenshot of waveform results here*

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|  |

## Assessment Rubrics

**Marks Distribution:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  | **LR2**  **Code** | **LR5**  **Results** | **LR7**  **Viva (Performance)** | **LR9**  **Report** |
| **In-lab** | **Task a** | 10 points | 10 points | 10 points | 20 Points |
| **Task b** | 10 points | 10 points |
| **Exercise (In-Lab)** |  | 20 points | 10 Points |
|  |  | 40 | 30 | 10 | 20 |
| **Total** |  | | | | 100 Points |

**Marks Obtained:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  | **LR2**  **Code** | **LR5**  **Results** | **LR7**  **Viva (Performance)** | **LR9**  **Report** |
| **In-lab** | **Task a** |  |  |  |  |
| **Task b** |  |  |
| **Exercise (In-Lab)** |  |  |  |
| **Total** |  | | | |  |